Remarks

The present amendment is submitted in response to the pending Office Action of November 11, 2001, in which claims 1-4, 9, 10, and 12-19 stand rejected, claims 5-8, 11, 20, and 20 stand objected to, and claims 22-43 stand withdrawn from consideration.

In reviewing their specification, Applicants suggest the amendment set forth herein to their specification to prevent any potential confusion regarding their use of a shorthand for setting forth concentrations in powers of 10 in Table 1 and in several other places. That is, while Applicants respectfully submit that such amendment is not required for patentability reasons, in that their specification as filed meets the statutory and regulatory requirements for invention descriptions in patent applications (c.f. there is no pending 112 rejection of record), Applicants suggest the proffered amendment to their specification to avoid any potential confusion.

In addition, in reviewing the drawing as submitted 27 August 2001, Applicants have noted an error in Fig. 1A. The reference line from 16' should lead to the curve immediately above curve 16, rather than leading to the curves 17, 18, 17A that have other reference numerals. The proposed drawing correction is enclosed herewith, with the proposed change indicated in red pen.

Finally, in the claims, Claims 5 and 11 have been rewritten to directly incorporate the limitations of their respective base claims, and the base claims have been cancelled. The other pending claims have been amended to redirect their dependencies respectively.

The above-described amendments are further indicated on the attached sheets entitled "Version with Markings to Show Changes Made."

Accordingly, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments, questions, or suggestions, please do not hesitate to contact the undersigned attorney at the telephone number and/or email address set forth below.

Respectfully submitted,

For: Furukawa et al.

By: _____

Mark F. Chadurjian
Reg. No. 30,739
Telephone: (802) 769-8843
Facsimile (802) 769-8938
Email: mchadurj@us.ibm.com

Exhibit A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Amend the paragraph that starts at page 4, line 14 (bridging to page 5) to read as follows:

Halo, or pocket, implants are well known as a means of moderating short-channel effects in very short MOSFETs. Short channel effects include Vt lowering and subthreshold slope increase as gate length decreases. Halo formation is usually accomplished by implanting a dopant type opposite to the source/drain doping, (e.g. by implanting boron in NFETs). A high energy is used for the halo implant to move it under the gate beyond the extent of the source/drain extension implant, which usually have significantly lower energies and higher doses, as shown in Table 1. As a result the p- dopant of the halo is often placed deeper than the n-dopant of the source/drain diffusion. The n-type source drain diffusion is thus decorated with a p-type halo all around. While the p-type dopant in the channel region is helpful for short channel effect, the halo extending under the source/drain has the unfortunate effect of increasing source/drain junction capacitance. Note that in the description below, the phrase "(#) e (#)" is a shorthand notation for concentrations in powers of ten; thus, e.g. in the table below, "1e13" means $1x10^{13}$.

In the claims:

5. (Amended) [The] An FET [as recited in claim 1, further] comprising:

a gate having a top and bottom portion, the top portion having a width that is greater than the width of the bottom portion;

a first diffusion self-aligned to the bottom portion; and

a second implant defined by said top portion.

7. (Amended) The FET as recited in claim 7 [1], further comprising a spacer adjacent said top portion and a third implant defined by said spacer.

10. (Amended) The FET of claim 11 [9], wherein said first conductive material is on a gate dielectric and said gate dielectric is on a substrate.

11. (Amended) An FET comprising a gate, said gate comprising a first conductive material and a second conductive material different from said first conductive material, said second conductive material being disposed on said first conductive material, said second conductive material extends beyond said first conductive material to provide a T-shaped gate [The FET of Claim 9], and wherein said first material has a dimension less than a photolithographic minimum dimension.

12. (Amended) The FET of claim 11 [9], wherein said first material comprises a first semiconductor material.

15. (Amended) The FET of claim 11 [9], wherein said second conductive material comprises polysilicon.

16. (Amended) The FET of claim 11 [9], wherein said first conductive material comprises polysilicon.

19. (Amended) The FET of claim 11 [9], wherein said second conductive material comprises a silicide.

20. (Amended) The FET of claim 11 [9], further comprising a spacer along sidewalls of said second conductive material.